REMARKS

Claims 1-19 are pending in the application. In response the office action, applicants have amended claims 6 and 7. Claims 1-19 remain pending for reconsideration.

Claims 6 and 7 have been amended editorially, for reasons not related to patentability, to improve the claim language.

Claims 1-4, 6-9, and 14-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,933,627 (Parady) in further view of U.S. Patent No. 5,881,277 (Bondi). Applicants respectfully traverse this rejection for the following reasons.

Applicants have previously pointed out that the various components of Parady relied upon in the rejection are not coupled together in a manner that reads on the claims. In response, the office action admits that there a other components between the various relied upon components, but relies on the use of "comprising" in the preamble to maintain that notwithstanding the numerous intervening components, the relied upon components are coupled to each other. This reading of the claim and the reference is simply incorrect. While "comprising" is open claim language, it does not operate to negate the recited inter-relationship of the claim elements. Particularly from the view of the claim as whole, the structure and inter-relationships of the components in Parady are different from and do not teach or suggest the recited modules and inter-relationship of the modules as recited in claim 1.

The office action asserts Parady teaches a "switch logic module (112 of Fig. 3) coupled to said state module, wherein said switch logic module detects a long-latency event in a software thread and schedules a switch to another thread during a latency of said long-latency event (see Col. 3, lines 57-65)." This is an incorrect reading of the reference. For the Examiner's convenience, the relied upon portion follows:

> Thread switching logic 112 is provided to give a hardware thread-switching capability. The indication that a thread switch is required is provided on line 114 providing an L2-miss indication from cache control/system interface 22 of Fig. 1. Upon such an indication, a switch to the next thread will be performed, using, in one embodiment, the next thread pointer on line 116. The next thread pointer is 2 bits indicating the next thread from an instruction which caused the cache miss.

The office action's analysis fails for several reasons. First, the thread switching logic 112 does not detect the long-latency event, it merely responds to a L2-miss signal. In other words, whatever logic the thread switching logic 112 has, it lacks the logic to detect the event. Instead, it appears that the logic of the thread switching logic 112 is devoted to decoding the next thread. To the extent that the Examiner wishes to broaden his net to catch whatever further logic generated the L2 miss signal, applicants note that such further logic is not coupled to the relied upon register files 48, 50, and 110.

Moreover, the thread switching logic 112 does not schedule switches, it merely performs them (see above: "Upon such an indication, a switch to the next thread will be performed"). Parady does not teach or suggest that the thread switching logic 112 schedules thread switches or, if it did, that such switches would be scheduled during the latency of the long latency event.

Because the office action's analysis is incorrect, and because Parady fails to teach or suggest even a switch logic module communicatively coupled to said state module, wherein said switch logic module detects an event in a software thread and schedules a switch to another software thread during a latency of said event, the office action fails to establish a prima facie case of obviousness.

The office action further admits that Parady fails to teach or suggest the recited switch logic module that detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of said mispredicted branch. In fact, Parady does not even mention and is not concerned with the problem of latency of mispredicted branches. Accordingly, there does not appear to be motivation to modify Parady to address this problem.

In any event, the office action relies on Bondi for this missing teaching. However, the office action merely cites a portion of Bondi which identifies a problem in connection with a pipelined processor (col. 1, lines 47-64). The office action fails to identify any portion of Brondi which allegedly teaches or suggests modifying Parady in any way which might bear on the claims.

In fact, the technique discussed in Brondi for addressing the misprediction problem in a pipelined processor does not appear to have any bearing on the present claims. Applicants submit that Bondi is directed to reducing the latency time of a mispredicted branch, and not to switching to another thread during such latency (e.g. see col. 16, lines 13-17).

The office action clarifies that the Examiner's position is that Bondi provides motivation to modify Parady because Parady deals with long latency events and Bondi allegedly teaches that mispredicted branches are long latency events. However, the combination still fails to establish a prima facie case of obviousness because even, assuming for the sake of argument, that Bondi provides motivation to modify Parady, it fails to teach or suggest how to modify Parady in a manner that might read on the claims.

In any event, Bondi fails to make up for the above-noted deficiencies in Parady.

In view of the structural elements missing from Parady, the lack of motivation to combine the references, and the missing teachings from both references, the office action fails to establish a prima facie case of obviousness of claim 1, and claim 1 is patentable over the cited combination of references. In particular, the combination of the references fails to teach or suggest at least the recited switch logic module coupled to said state module, wherein said switch logic module detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of said mispredicted branch. Claims 2-7 depend either directly or indirectly from claim 1 and are therefore also patentable.

With respect to claim 2, the office action is incorrect in asserting that the logic 112 detects anything in the software threads. Accordingly, claim 2 is separately patentable.

With respect to claim 3, the office action is incorrect in its assertion. The cited portion is silent with respect to resetting the L2-miss signal when the switch is completed. Accordingly, claim 3 is separately patentable.

With respect to claim 4, the office action admits that the recited outstanding switch request indicator is completely absent from the references, but argues that such a signal must be inherent. This is incorrect. First, although not relevant to the claim, any of a number of mechanisms may be utilized to handle the example given in the office action, none of which are inherent. Accordingly, the recited outstanding switch request indicator is not inherent in Parady. Moreover, as noted above, the logic 112 does not schedule the switches, it merely performs them. Accordingly, it does not teach or suggest the need for an outstanding switch request indicator. Accordingly, claim 4 is separately patentable.

Applicants strenuously object to the Examiner's characterization of claims 8 and 14 in paragraph 12 of the action as being 'nearly identical' or 'encompassing the same scope' as compared to claim 1. Applicants further objects to similar statements made with respect to other

claims throughout the action. Each claim stands on its own and may encompass different and / or broader scope.

With respect to claims 8 and 14, the office action fails to comply with 37 C.F.R. § 104 (c)(2) because the office action fails to sufficiently designate the particular part of each reference relied upon for disclosing each claim recitation, so that a full and fair analysis and response may be made. In fact, the office action fails completely to establish how the references might be read on the claims. Claims 8 and 14 each recite:

> detecting a switching event in a software thread;
>
> determining whether a mispredicted branch has been detected in said software thread; and
>
> executing a switch to another software thread during a latency of said mispredicted branch if said mispredicted branch has been detected.

Even upon casual inspection it is apparent that the scope of claim 1 and claims 8 and 14 are not 'nearly identical'. Applicants cannot respond to a rejection that has not been made. If the rejection is maintained, or if new rejections are made, applicants respectfully request a new non-final action in compliance with 37 C.F.R. § 104 (c)(2). In particular applicants respectfully request that the Examiner set forth the particular portion relied upon for teaching detecting a switching event in a software thread and determining whether a mispredicted branch has been detected in said software thread.

In the absence of a legally sufficient rejection, the office action fails to establish a prima facie case of obviousness with respect to claims 8 and 14, and claims 8 and 14 are patentable over the cited combination of references. The respective dependent claims 9-13 and 15-19 are likewise patentable.

Claims 5, 10-13 and 16-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Parady, in further view of Brondi, and in further view of U.S. Patent No. 6,567,839 (Borkenhagen). Applicants respectfully traverse this rejection for the following reasons.

Borkenhagen, which is relied upon for various teachings admitted to be missing from Parady and Brondi, fails to make up for the above noted deficiencies with the other references. Accordingly, the office action fails to establish a prima facie case of obviousness with respect to the rejected claims.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If the rejections are to be maintained, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below to arrange a personal interview.

Respectfully submitted,

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Date

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